Correct-by-design Control Synthesis for Multilevel Converters using State Space Decomposition

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High-power converters based on elementary switching cells are more and more used in the industry of power electronics owing to various advantages such as lower voltage stress and reduced power loss. However, the complexity of controlling such converters is a major challenge that the power manufacturing industry has to face with. The synthesis of industrial switching controllers relies today on heuristic rules and empiric simulation. The state of the system is not guaranteed to stay within the limits that are admissible for its correct electrical behavior. We show here how to apply a formal method in order to synthesize a correct-by-design control that guarantees that the power converter will always stay within a predefined safe zone of variations for its input parameters. The method is applied in order to synthesize a correct-by-design control for 5-level and 7-level power converters with a flying capacitor topology. We check the validity of our approach by numerical simulations for 5 and 7 levels. We also perform physical experimentations using a prototype built by SATIE laboratory for 5 levels.

1 Introduction

Switched control has gained much attention recently due to its property of being easily implemented, especially in the field of power converters. Power converters play an important role in the field of renewable energy: they are used to connect renewable sources to powergrids, optimize the efficiency of solar panels and wind generators (see, e.g., [1]). In some topologies, there is however a dramatic increase of the number of switches, which entails an increasing number of degrees of freedom, and complicates the controller design . There is therefore a niche of application for formal methods in order to produce correct-by-design control methods. The general function of a multilevel power converter is to synthesize a desired voltage from several levels of DC voltage. For this reason, multilevel power converters can easily provide the high power required by large electric drive systems. A multilevel converter is a power converter made of capacitors and switching cells (as well as opposite switching cells which are in complementary positions);

In this paper, we consider the design of control policies for power converters with a number of levels $\ell = 5$ and $\ell = 7$. A multilevel converter for $\ell = 5$ is schematized on Figure 1. According to the positions of the cells, one is able to fraction the load voltage. By controlling the global position of the switches during a simple fixed time-stepping procedure, it is then possible to generate a staircase voltage with levels that approximates a triangular or a sinusoidal waveform (see Figure 2, for 5 levels).

The problem which arises is to select the appropriate switching control strategy among a number of combinations of switch positions which increases exponentially with the number of levels (and pairs of switches). A crucial difficulty comes from the fact that, in order to be admissible, the control of the switching cells must guarantee that the voltages across the cell-capacitors are constrained within a certain

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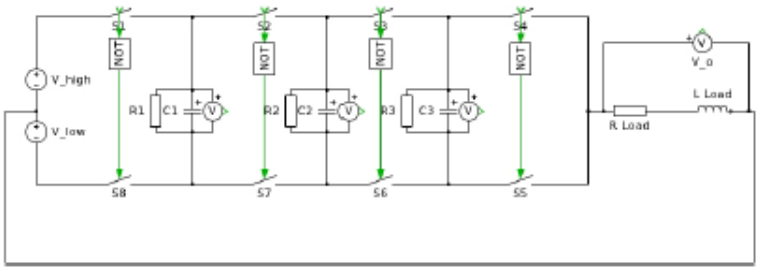


Figure 1: Electrical scheme of a 5-level flying capacitor converter

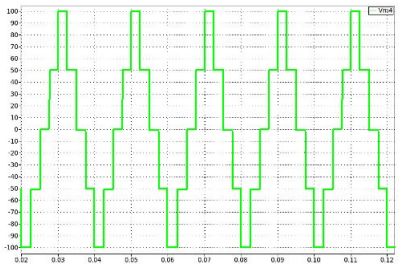


Figure 2: Staircase output voltage waveform for a 5-level converter

range defined by the device blocking voltage rating. The control must thus guarantee a *safety property*, called "capacitor voltage balancing": the voltage of each individual capacitor should stay inside a limited predefined interval. The synthesis of industrial switching controllers relies today on heuristic rules and empiric simulation. The state of the system is not guaranteed to always satisfy capacitor voltage balancing. In this paper, we show how to synthesize a control, by applying a formal method, called *state space decomposition procedure* [4]. The synthesized control is "correct-by-design" because it is ensured to make the electrical state parameters of the system stay within predefined safe zones of variations. Numerical simulations, performed at levels $\ell = 5, 7$, confirm the safety properties of the synthesized control. Physical experimentations are also successfully performed on a prototype built by SATIE Electronics Laboratory, at level $\ell = 5$.

Outline of the paper

In Section 2, we present the principles of the state space decomposition method. In Section 3, we apply the method in order to synthesize the control of multilevel converters with a flying capacitor topology, for 5 and 7 levels. In Section 4, we present physical experimentations done with a prototype of 5-level converter. We conclude in Section 5.

2 State Space Decomposition Method

A multilevel converter can be seen as a "switched system", where the different operating modes depend on the positions of the switching cells. In this section, we describe a general method that is useful for proving properties of switched systems. The method will be subsequently applied to multilevel converters in Section 3.

2.1 Model of affine sampled switched systems

A *switched system* Σ is defined by a finite family of differential equations of the form $\{\dot{x} = f_u(x)\}_{u \in U}$ where U is a finite set of *modes* (see, e.g., [5, 14]). In the following, we consider that the dynamics of the subsystems are *affine* (i.e., $f_u(x)$ is of the form $A_u x + b_u$ with $A_u \in \mathbb{R}^{n \times n}$ and b_u a vector of $\mathbb{R}^n$). The control problem for a switched system Σ is to find a piecewise constant law $\mathbf{u} : \mathbb{R}_{\geq 0} \to U$ in order to achieve some pertained goals. The *switching instants* are the times at which $\mathbf{u}$ changes its value. An *affine sampled switched system* is a switched system for which the switching instants occur at integer multiples of τ (called *sampling parameter*). We will use $\mathbf{x}(t,x,u)$ to denote the point reached by Σ at time t under mode u from the initial condition x. This gives a transition relation $\to_u^\tau$ defined for x and x' in $\mathbb{R}^n$ by: $x \to_u^\tau x'$ iff $\mathbf{x}(\tau,x,u) = x'$. Given a set $X \subset \mathbb{R}^n$, we define:

$$Post_u(X) = \{x' \mid x \to_u^\tau x' \text{ for some } x \in X\}.$$

It can be seen that $Post_u(X)$ is the result of an affine transformation of the form $C_u X + d_u$ with $C_u \in \mathbb{R}^{n \times n}$ and d_u a vector of $\mathbb{R}^n$.

A *pattern* π is defined as a finite sequence of modes. A *k-pattern* is a pattern of length at most k. The mapping $Post_\pi$ is itself an affine transformation.

Given a pattern π of the form $(u_1 \cdots u_m)$, and a set $X \subset \mathbb{R}^n$, the *unfolding of X via π*, denoted by $Unf_\pi(X)$, is the set $\bigcup_{i=0}^m X_i$ with:

- $X_0 = X$,
- $X_{i+1} = Post_{u_{i+1}}(X_i)$, for all $0 \leq i \leq m-1$.

The unfolding thus corresponds to the set of all the intermediate states produced when applying pattern π to the states of X.

2.2 Safety control problem

A safety property is typically expressed using a subset S of the continuous state space, called *safe set*. In a simple formulation, S is a *box*, i.e., a cartesian product of intervals that specify the minimum and maximum values tolerated for each state component. Given a safe set S, and a domain of interest $R \subseteq S$, we can define the notion of "safe control" in this context as follows.

Definition 1 *Given a domain of interest R and safe set S with $R \subseteq S$, a* safe control of R w.r.t. S *is a function that associates to each $x \in R$ a pattern π such that:*

- $Post_\pi(\{x\}) \subseteq R$, *and*
- $Unf_\pi(\{x\}) \subseteq S$.

Given a domain of interest R and a set S with $R \subseteq S$, the safety control problem consists in finding a safe control of R w.r.t. S. In [4], in order to solve such a problem, we introduced the notion of "(safe) decomposition".

Definition 2 *Given a set $R \subset \mathbb{R}^n$ and a set S with $R \subseteq S$, a* safe decomposition of R w.r.t. S *is a set Δ of the form $\{V_i, \pi_i\}_{i \in I}$, where I is a finite set of indices, V_is are subsets of R, π_is are k-patterns, such that:*

- $\bigcup_{i \in I} V_i = R$,
- *for all $i \in I$: $Post_{\pi_i}(V_i) \subseteq R$, and*
- *for all $i \in I$: $Unf_{\pi_i}(V_i) \subseteq S$.*

A decomposition $\Delta = \{(V_i, \pi_i)\}_{i \in I}$ naturally induces a *state-dependent control* on R. Furthermore, the controlled trajectories starting from R never leave S. Indeed, given a starting state x_0 in R, we know that $x_0 \in V_i$ for some $i \in I$ (since $R = \bigcup_{i \in I} V_i$); one thus applies π_i to x_0, which gives a new state x_1 that belongs itself to R (since $Post_{\pi_i}(V_i) \subseteq R$); furthermore, since $Unf_{\pi_i}(V_i) \subseteq S$, all the intermediate states produced by application of π_i are guaranteed to belong to S. The process can then be repeated on x_1, and so on iteratively. Formally, we have:

Proposition 1 *Suppose that Δ is a safe decomposition of R w.r.t. S. Then the control of R induced by Δ is safe w.r.t S.*

The problem of finding a safety controller thus reduces to the problem of finding a safe decomposition Δ. The latter problem can be solved by using the *state space decomposition method* [4], as explained below.

2.3 State space decomposition method

We give here a simple algorithm, adapted from [4], called Decomposition algorithm. Given a set R and a set S with $R \subseteq S$, the algorithm outputs, when it succeeds, a decomposition Δ of R w.r.t S, of the form $\{V_i, \pi_i\}_{i \in I}$. The input sets R and S are given under the form of *boxes* of $\mathbb{R}^n$ (i.e., cartesian products of n closed intervals). The subsets V_is of R are boxes that are obtained by repeated bisection. At the beginning, the Decomposition procedure calls sub-procedure Find_Pattern in order to get a k-pattern π such that $Post_\pi(R) \subseteq R$ and $Unf_\pi(R) \subseteq S$. If it succeeds, then it is done. Otherwise, it divides R into 2^n sub-boxes $V_1, \ldots, V_{2^n}$ of equal size. If for each V_i, Find_Pattern gets a k-pattern π_i such that $Post_{\pi_i}(V_i) \subseteq R$ and $Unf_{\pi_i}(V_i) \subseteq S$, it is done. If, for some V_j, no such pattern exists, the procedure is recursively applied to V_j. It ends with success when a safe decomposition of R w.r.t. S is found, or failure when the maximal degree d of decomposition is reached. The algorithmic form of the procedure is given in Algorithms 1 and 2. (For the sake of simplicity, we consider the case of dimension $n = 2$, but the extension to $n > 2$ is straightforward.) The main procedure Decomposition(W, R, S, D, K) is called with R as input value for W, d for input value for D, and k as input value for K; it returns either $\langle \{(V_i, \pi_i)\}_i, True \rangle$ with $\bigcup_i V_i = W$, $\bigcup_i Post_{\pi_i}(V_i) \subseteq R$, $\bigcup_i Unf_{\pi_i}(V_i) \subseteq S$ or $\langle \_, False \rangle$. Procedure Find_Pattern(W,R,S,K) looks for a K-pattern π for which $Post_\pi(W) \subseteq R$ and $Unf_\pi(W) \subseteq S$: it selects all the K-patterns by non-decreasing length order until either it finds such a pattern π (output: $\langle \pi, True \rangle$), or none exists (output: $\langle \_, False \rangle$). The correctness of the procedure is stated as follows.

Theorem 1 *If Decomposition(R,R,S,d,k) returns $\langle \Delta, True \rangle$, then Δ is a safe decomposition of R w.r.t. S.*

In [4], we have developed a tool that implements the Decomposition procedure, using zonotopes [6], and is written in Octave [10]. We now describe the application of this tool, called MINIMATOR [9], for synthesizing controllers of multilevel converters.

3 Application to Multilevel Converters

3.1 Multilevel converters as switched systems

There are different possible topologies for multilevel power converters: neutral-point clamped, cascaded H-bridge, Modular Multilevel Converter (see e.g., [12, 2, 7, 8]). We focus here on the flying capacitor topology [8]. The electrical scheme of a 5-level converter was given in Figure 1. There are 4 pairs of switching cells S_1, S_2, S_3, S_4 (the high-side switch conducting position is indicated by 1 and the lowside switch conducting position by 0), and 3 capacitors C_1, C_2, C_3. The state of the system is $x(t) = [v_1(t)\ v_2(t)\ v_3(t)\ i(t)]^T$ where $v_j(t)$ is the voltage across C_j ($1 \leq j \leq 3$) and $i(t)$ is the current flowing in the circuit. The duration of a cycle is $T = 8\tau$. The *mode* of the system is characterized by the

Algorithm 1: Decomposition(W, R, S, D, K)

Input: A box W, a box R, a box S, a degree D of decomposition, a length K of pattern
Output: $\langle \{(V_i, \pi_i)\}_i, True \rangle$ with $\bigcup_i V_i = W$, $\bigcup_i Post_{\pi_i}(V_i) \subseteq R$ and $\bigcup_i Unf_{\pi_i}(V_i) \subseteq S$ or $\langle \_, False \rangle$

$(\pi, b) := Find\_Pattern(W, R, S, K)$
if $b = True$ **then**
  return $\langle \{(W, \pi)\}, True \rangle$
else
  if $D = 0$ **then**
    return $\langle \_, False \rangle$
  else
    Divide equally W into $(W_1, \cdots, W_{2^{n-2}})$
    for $i = 1 \ldots 2^{n-2}$ **do**
      (Δ_i, b_i) := Decomposition(W_i,R,S,$D-1$,K)
    return $(\bigcup_{i=1\ldots 2^{n-2}} \Delta_i, \bigwedge_{i=1\ldots 2^{n-2}} b_i)$

Algorithm 2: Find_Pattern(W, R, K)

Input: A box W, a box R, a box S a length K of pattern
Output: $\langle \pi, True \rangle$ with $Post_\pi(W) \subseteq R$ and $Unf_\pi(W) \subseteq S$, or $\langle \_, False \rangle$ when no pattern maps W into R

for $i = 1 \ldots K$ **do**
  $\Pi :=$ set of patterns of length i
  while Π *is non empty* **do**
    Select π in Π
    $\Pi := \Pi \setminus \{\pi\}$
    if $Post_\pi(W) \subseteq R$ *and* $Unf_\pi(W) \subseteq S$ **then**
      return $\langle \pi, True \rangle$
return $\langle \_, False \rangle$

value (0 or 1) of the switching cells, i.e., by the value of vector $S = [S_1\ S_2\ S_3\ S_4]^T$.[1] There are thus $2^4 = 16$ modes. A mode S induces an output voltage v_o of value $\Sigma_{j=1}^{3}(S_{j+1} - S_j)v_j + S_1 v_{high} - (1 - S_1)v_{low}$, where v_{low} and v_{high} are the input voltages of low level and high level respectively. For the sake of simplicity, we suppose: $v_{high} = v_{low} = v_{input}$. The system then outputs 5 different levels of voltage which go from $-v_{input}$ up to $+v_{input}$ with steps at $-\frac{v_{input}}{2}, 0, \frac{v_{input}}{2}$. The ideal value v_i^* of the voltage across capacitor C_i ($1 \leq i \leq 3$) depends on the values of v_{input}. Here we use: $v_{input} = 100V$, and $v_1^* = 150V$, $v_2^* = 100V$, $v_3^* = 50V$. The 5-level converter can be seen as a switched system. Given a mode S, the associated dynamics is of the form $\dot{x}(t) = A_S x(t) + b_S$ with:

$$A_S = \begin{pmatrix} -\frac{1}{R_1 C_1} & 0 & 0 & \frac{S_1 - S_2}{C_1} \\ 0 & -\frac{1}{R_2 C_2} & 0 & \frac{S_2 - S_3}{C_2} \\ 0 & 0 & -\frac{1}{R_3 C_3} & \frac{S_3 - S_4}{C_3} \\ \frac{S_2 - S_1}{L_{Load}} & \frac{S_3 - S_2}{L_{Load}} & \frac{S_4 - S_3}{L_{Load}} & -\frac{R_{Load}}{L_{Load}} \end{pmatrix} \text{ and } b_S = \begin{pmatrix} 0 \\ 0 \\ 0 \\ \frac{(2S_1 - 1)v_{input}}{L_{Load}} \end{pmatrix}$$

By controlling the modes at each sampling time, one can synthesize a 5-level staircase function. Not all the transitions between modes are admissible: we allow to switch only one (pair of) cell(s) at a time.

[1] Besides, we have: $S_5 = \neg S_1$, $S_6 = \neg S_2$, $S_7 = \neg S_3$ and $S_8 = \neg S_4$.

The graph of admissible transitions during a cycle is depicted in Figure 3. The nodes of the graph are labeled by the modes. Each path represents a possible pattern for one cycle, leading from voltage $-v_{input}$ (mode 0000) to voltage $+v_{input}$ (mode 1111) through voltages $-\frac{v_{input}}{2}$, 0, $\frac{v_{input}}{2}$ then back to voltage $-v_{input}$ (mode 0000) through voltages $\frac{v_{input}}{2}$, 0, $\frac{v_{input}}{2}$. There are thus 576 possible patterns for generating a 5-level staircase signal on one cycle.

We explain in the following how to apply the tool MINIMATOR in order to find a safe decomposition involving these patterns.

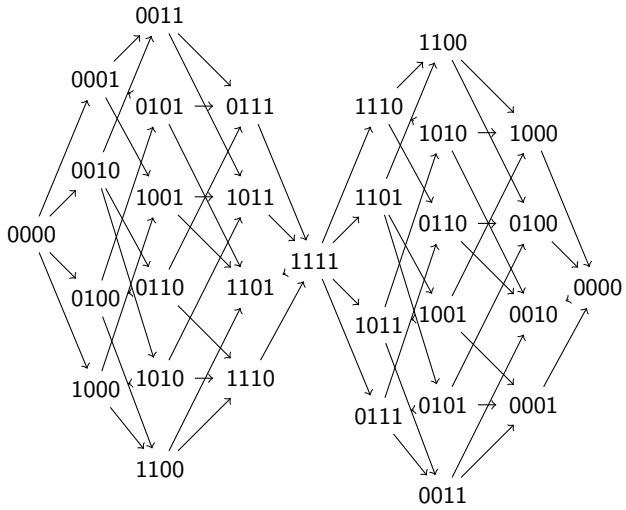


Figure 3: Transition graph corresponding to a cycle of 5-level staircase signal

3.2 Application of the Decomposition procedure to a 5-level converter

We consider the following numerical values of the electrical parameters: $v_{input} = 100$V, $R_{Load} = 50\Omega$, $C_1 = C_2 = C_3 = 0.0012$F, $L_{Load} = 0.2$H, $R_1 = R_2 = R_3 = 20,000\Omega$, $T = 8\tau = 0.02s$ (which corresponds to a frequency of 50Hz).

In this context, a 5-level converter outputs ideally a staircase waveform with an amplitude of 200V, centered around 0V. We consider that a variation of $\pm 5V$ is admissible as it represents a variation of 10% on the least charged capacitor C_3. It is interesting to notice that at each beginning of a cycle the value of i is null. This suggest to look for a state-dependent control which depends only on the capacitor voltages v_1, v_2, v_2, and not on the value of i. We will thus focus on the voltage dimensions of the control box R and disregard its intensity dimension. For R, we take $R = [145,155] \times [95,105] \times [45,55]$, which corresponds to a product of intervals centered around the ideal values with a variation of $\pm 5V$ (i.e., 10% of the least charged capacitor C_3). For S, we take $R + \varepsilon$ with $\varepsilon = 1V$, which means that we have an additional tolerance of $\pm 1V$ for the fluctuations occurring between two beginnings of cycle.

Given $R = [145,155] \times [95,105] \times [45,55]$ and $S = [144,156] \times [94,106] \times [44,56]$, we perform the procedure of Decomposition, implemented in MINIMATOR tool, on a machine equipped with an Intel core2 CPU X6800 at 2.93GHz and with 2GiB of Ram memory. With parameters $d = 1$ and $k = 8$, the procedure outputs in 60 seconds a decomposition $\Delta = \{(V_i, \pi_i)\}_{i=1,\ldots,8}$ with:

- $V_1 = [145,150] \times [95,100] \times [45,50]$
- $V_2 = [145,150] \times [95,100] \times [50,55]$
- $V_3 = [145,150] \times [100,105] \times [45,50]$

- $V_4 = [145,150] \times [100,105] \times [50,55]$
- $V_5 = [150,155] \times [95,100] \times [45,50]$
- $V_6 = [150,155] \times [95,100] \times [50,55]$
- $V_7 = [150,155] \times [100,105] \times [45,50]$
- $V_8 = [150,155] \times [100,105] \times [50,55]$

and

- π_1: $(0000 \to 0001 \to 0101 \to 1101 \to 1111 \to 1101 \to 0101 \to 0001 \to 0000)$
- π_2: $(0000 \to 0100 \to 0101 \to 1101 \to 1111 \to 1101 \to 0101 \to 0100 \to 0000)$
- π_3: $(0000 \to 0001 \to 0011 \to 1011 \to 1111 \to 1011 \to 0011 \to 0001 \to 0000)$
- π_4: $(0000 \to 0010 \to 0011 \to 1011 \to 1111 \to 1011 \to 0011 \to 0010 \to 0000)$
- π_5: $(0000 \to 1000 \to 1010 \to 1110 \to 1111 \to 1110 \to 1010 \to 1000 \to 0000)$
- π_6: $(0000 \to 1000 \to 1100 \to 1101 \to 1111 \to 1101 \to 1100 \to 1000 \to 0000)$
- π_7: $(0000 \to 0100 \to 0110 \to 0111 \to 1111 \to 0111 \to 0110 \to 0100 \to 0000)$
- π_8: $(0000 \to 1000 \to 1010 \to 1011 \to 1111 \to 1011 \to 1010 \to 1000 \to 0000)$

By Proposition 1, the control of R induced by Δ is safe w.r.t. S: under the control induced by Δ, all the trajectories starting from R always stay in S. This guarantees that the property of capacitor voltage balance is satisfied. We present in Figures 4 and 5 a numerical simulation of this controller on the system starting from the point $v_1(0) = 150V, v_2(0) = 100V, v_3(0) = 50V$ and $i(0) = -3A$. This simulation has been performed using tool PLECS [11]. One can check on the simulation that the system state always stays inside S.

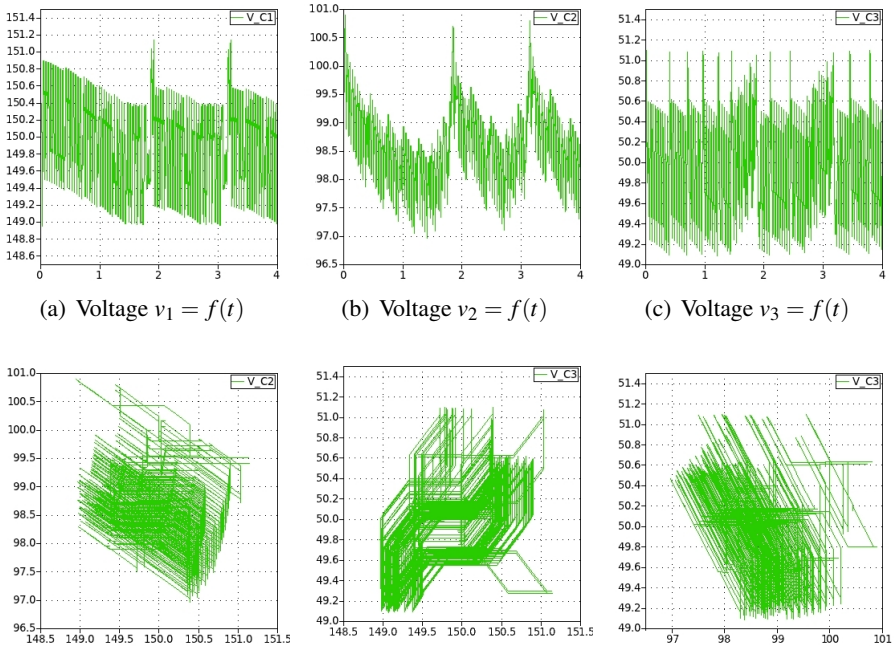
3.3 Application of the Decomposition procedure to a 7-level converter

We now consider the case of an ℓ-level converter with $\ell = 7$. There are now 6 pairs of switching cells and 5 capacitors $C_1, \ldots, C_5$. The state of the system is $x(t) = [v_1(t)\ v_2(t)\ v_3(t)\ v_4(t)\ v_5(t)\ i(t)]^T$ where $v_j(t)$ is the voltage across C_j ($1 \leq j \leq 5$) and $i(t)$ is the current flowing in the circuit. The generated waveform now goes from $-v_{input}$ up to $+v_{input}$ with steps at $-\frac{2}{3}v_{input}$, $-\frac{1}{3}v_{input}$, 0, $\frac{1}{3}v_{input}$, $\frac{2}{3}v_{input}$, and the cycle duration is $T = 12\tau$. There are now $518,400$ possible patterns for generating an 7-level staircase signal on 1 cycle. We used the following values for the system constants: output at 50Hz,[2] capacitances of $0.1F$, resistor values 50Ω, inductor values $0.137H$, $v_{input} = 300V$. Ideally, the output is thus a staircase waveform with an amplitude of 600V, centered around 0V, and the ideal values v_i^* of the capacitor voltages of the capacitor C_i are given by: $v_1^* = 500V$, $v_2^* = 400V$, $v_3^* = 300V$, $v_4^* = 200V$, $v_5^* = 100V$. For R, we take $R = [495,505] \times [395,405] \times [295,305] \times [195,205] \times [95,105]$, which corresponds to a product of intervals centered around the ideal values with a variation of $\pm 5V$ (i.e., 5% of the least charged capacitor C_5). For S, we take $R + \varepsilon$ with $\varepsilon = 1V$, which means that we have an additional tolerance of $\pm 1V$ for the fluctuations occurring between two beginnings of cycle. On the same machine as in Section 3.2, with parameters $d = 1$ and $k = 12$, MINIMATOR outputs in 98 minutes a decomposition Δ which is safe w.r.t. S. See [3] for more details.

We present in Figures 6 and 7 a numerical simulation of the controlled system starting from the point $v_1(0) = 500V$, $v_2(0) = 400V$, $v_3(0) = 300V$, $v_4(0) = 200V$, $v_5(0) = 100V$ and $i(0) = -2.5A$. One can check again on the simulation that the system state always stays inside S.

It is difficult to perform experiments with ℓ greater than 7 with the present implementation. The complexity of the state decomposition procedure is indeed exponential in the number ℓ of levels. We are presently implementing MINIMATOR on a parallel computing architecture (see [9]) in order to increase the tractable number of levels.

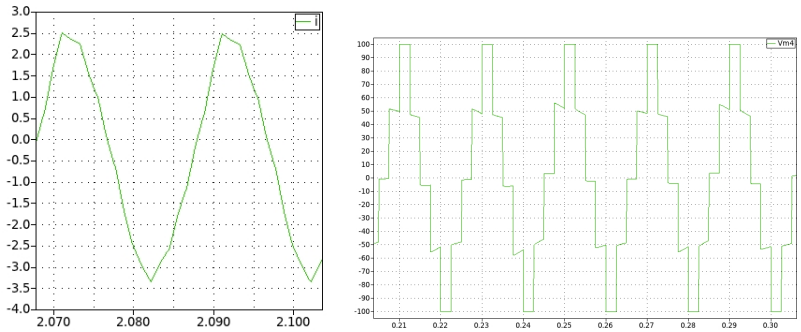
[2] which corresponds to $T = 12\tau = 0.02s$



(a) Voltage $v_1 = f(t)$ (b) Voltage $v_2 = f(t)$ (c) Voltage $v_3 = f(t)$

(d) Projection in plane (v_1, v_2) (e) Projection in plane (v_1, v_3) (f) Projection in plane (v_2, v_3)

Figure 4: Capacitor voltages



(a) Current i (b) Output voltage v_o

Figure 5: Current and output voltage

4 Physical Experimentations on a 5-level Converter

A prototype of the 5-level flying capacitor has been realized by the SATIE Laboratory in order to test our control strategy on an actual system. See Figure 8 for a picture of the prototype. Our control strategy was applied to the system via Simulink and a dSpace® interface. The results are presented in Figure 9 for the output voltage and the capacitor charges. In Figure 10, we present the same results but with a larger scale on the capacitor voltage to see the fluctuations around the reference values. As we can see, the experimental results are very closed to those obtained by simulation with PLECS of Section 3.2. In Figure 11, we represent the output voltage together with the current (after appropriate resizing) flowing the load. During the experimentations, we have successfully tested the robustness of the controller in presence of the following perturbations:

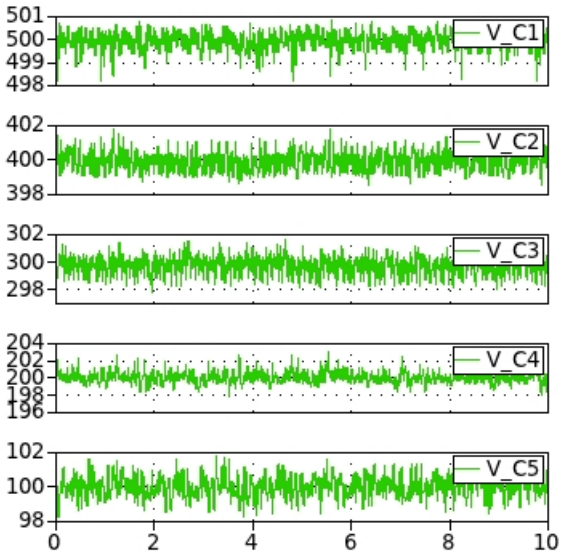
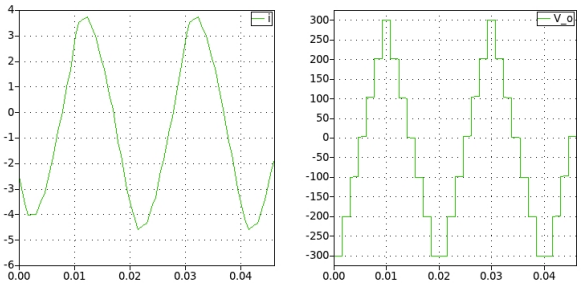


Figure 6: Capacitor voltages



(a) Current i (b) Voltage v_o

Figure 7: Current and output voltage

1. The ideal voltage source as input is no longer ideal but its values fluctuate around the reference value.
2. We use a time-varying period T of cycle (instead of a constant one), and check the preservation of the capacitor voltages balance. The result of this experiment is depicted in Figure 12.

Although these preliminary tests of robustness are promising, they need to be consolidated, in particular in presence of significant variations of resistor loads.

5 Final Remarks

We have synthesized a control strategy for a 5-level and a 7-level flying capacitor converters using the method of state space decomposition. This control is state-dependent and is interesting because:

- at each electrical cycle, the controller indicates all the subsequent switching modes needed to produce one period of the output voltage (instead of just the next switching mode),
- the controller takes into account only the capacitor voltages state and not the intensity state; this is interesting because for practical applications, a current sensor is not always desired (see [2]).

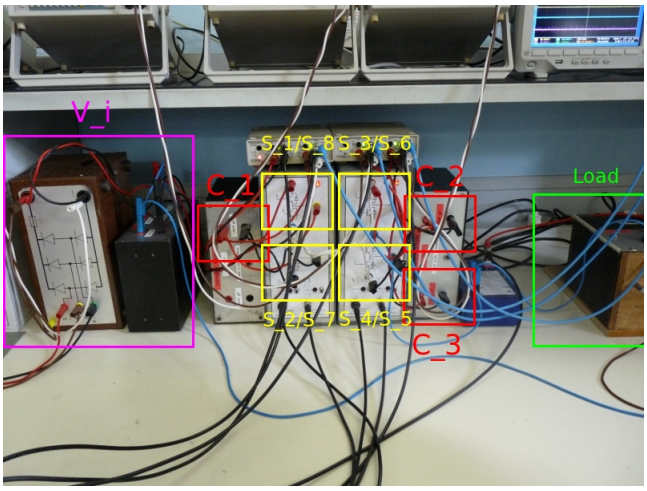


Figure 8: Prototype built by SATIE

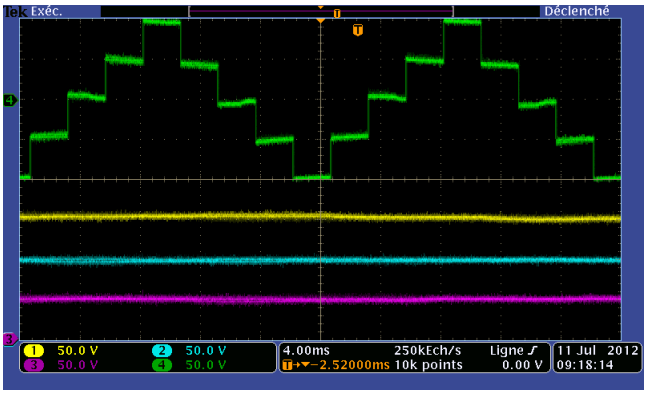


Figure 9: Output voltage (above in green) and capacitor voltages (below)

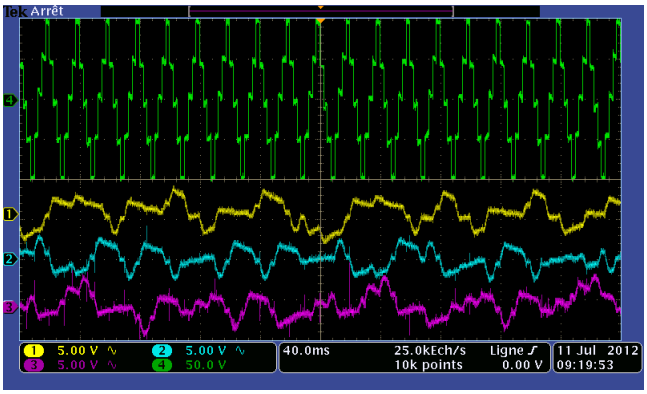


Figure 10: Zoom of output voltage (above) and capacitors voltages (below)

We have checked by numerical simulations and physical experimentations that the control satisfies the capacitor voltage balancing and the staircase shape of the output voltage. We have also checked the robustness of the method with respect to several sources of perturbation.

Figure 11: Output voltage (in green) and current (in yellow, after appropriate resizing) in the circuit

Figure 12: Output voltage (above) and capacitor voltages (below) in presence of time-varying period T

The method can be easily refined in order to generate sinusoidal-like output signals rather than the triangular-like output signals generated here: it suffices to adjust the switching instants within the period T of the cycle, instead of using uniformly τ.

The method can be applied in principle to any number of levels for the flying capacitor topology. However, it suffers from an exponential increase of complexity when the level ℓ grows: the method reaches its limit for $\ell = 9$, which corresponds to a dimension $n = 7$ of the state space.

For $\ell = 5, 7$, the Decomposition procedure is well-suited to the *flying capacitor* topology: the pattern length input k is $2 \times (\ell - 1)$ where ℓ is the number of levels of the converter, and the depth input d is 1, which means that the decomposition is found after a single bisection. Note however that such simple decompositions of the state space do not necessarily exist for other topologies: for multilevel modular converter toplogy [7], we had to propose in [13] a different and specialized algorithm which takes additionally into account the value of the intensity state.

In future work, we plan to improve the robustness of the decomposition method for flying capacitor topology under variations of the resistive and inductive load. This will allow us to model the time-varying load of electrical networks, which is a basic feature of electricity distribution, and a major challenge today for renewable-energy technologies. We are also implementing the tool MINIMATOR on a parallel computing architecture in order to synthesize correct-by-design controls for multilevel converters with a greater numbe ℓ of levels.

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References

[1] I. Cervantes, F.J. Perez-Pinal & A. Mendoza-Torres (2009): *Hybrid Control of DC-DC Power Converters*. In: *Renewable Energy (Chapter 10)*, T J Hammons, pp. 173,193, doi:10.5772/7370.

[2] Zhong Du, L.M. Tolbert, B. Ozpineci & J.N. Chiasson (2009): *Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter*. *IEEE Transactions on Power Electronics* 24(1), pp. 25–33, doi:10.1109/TPEL.2008.2006678.

[3] G. Feld, L. Fribourg, D. Labrousse, B. Revol & R. Soulat (2012): *Correct by design control of 5-level and 7-level converters*. Research Report LSV-12-25, Laboratoire Spécification et Vérification, ENS Cachan, France.

[4] Laurent Fribourg & Romain Soulat (2013): *Stability Controllers for Sampled Switched Systems*. In Parosh Aziz Abdulla & Igor Potapov, editors: *Proceedings of the 7th Workshop on Reachability Problems in Computational Models (RP'13)*, *Lecture Notes in Computer Science* 8169, Springer, Uppsala, Sweden, pp. 135–145, doi:10.1007/978-3-642-41036-9_13.

[5] A. Girard, G. Pola & P. Tabuada (2010): *Approximately Bisimilar Symbolic Models for Incrementally Stable Switched Systems*. *IEEE Trans. on Automatic Control* 55, pp. 116–126.

[6] W. Kühn (1998): *Zonotope dynamics in numerical quality control*. *Mathematical Visualization*, pp. 125–134, doi:10.1007/978-3-662-03567-2_10.

[7] A. Lesnicar & R. Marquardt (2003): *An innovative modular multilevel converter topology suitable for a wide power range*. In: *Power Tech Conference Proceedings, 2003 IEEE Bologna*, 3, pp. 6 pp. Vol.3–, doi:10.1109/PTC.2003.1304403.

[8] T.A. Meynard & H. Foch (1992): *Multi-level conversion: high voltage choppers and voltage-source inverters*. In: *23rd Annual IEEE Power Electronics Specialists Conference (PESC '92)*, 1, pp. 397–403, doi:10.1109/PESC.1992.254717.

[9] *MINIMATOR Web Page*. https://bitbucket.org/ukuehne/minimator/.

[10] *Octave Web Page*. http://www.gnu.org/software/octave/.

[11] *PLECS Web Page*. http://www.plexim.com.

[12] B. Singh, N. Mittal, K.S. Verma, D. Singh, S.P. Singh, R. Dixit, M. Singh & A. Baranwal (2012): *Multilevel inverter: A literature survey on topologies and control strategies*. *International Journal of Reviews in Computing* 10.

[13] Romain Soulat, Guillaume Hérault, Denis Labrousse, Bertrand Revol, Gilles Feld, Stéphane Lefebvre & Laurent Fribourg (2013): *Use of a full wave correct-by-design command to control a multilevel modular converter*. In Philippe Lataire, editor: *Proceedings of the 15th European Conference on Power Electronics and Applications (EPE'13)*, IEEE Power Electronics Society, Lille, France, pp. 1,8, doi:10.1109/EPE.2013.6634448. Available at `http://www.lsv.ens-cachan.fr/Publis/PAPERS/PDF/SHLRFLF-epe13.pdf`.

[14] Paulo Tabuada (2009): *Verification and Control of Hybrid Systems: A Symbolic Approach*, 1st edition. Springer Publishing Company, Incorporated.

[15] E. Zuazua (2005): *Propagation, observation, and control [15] of waves approximated by finite difference methods*. *SIAM Review* 47(2), pp. 197 –243.