Correct-by-Design Control Synthesis for Multilevel Converters using State Space Decomposition

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FSFMA, 13 May 2014

Plan

Context: Multilevel Converters

2-level Example: Boost DC-DC Converter

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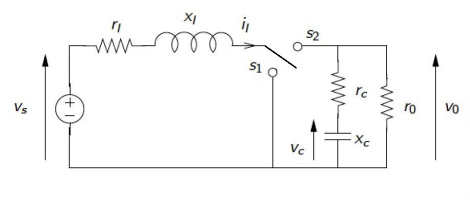

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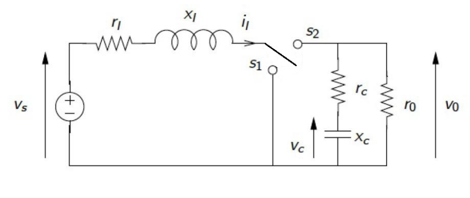

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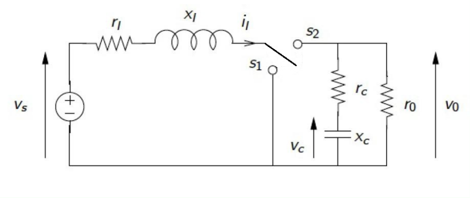

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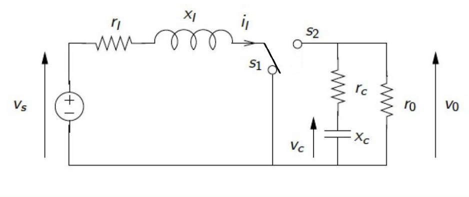

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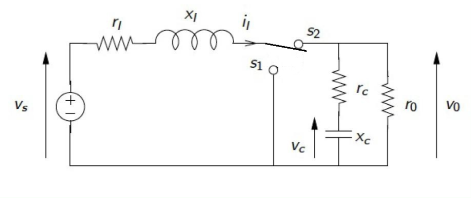

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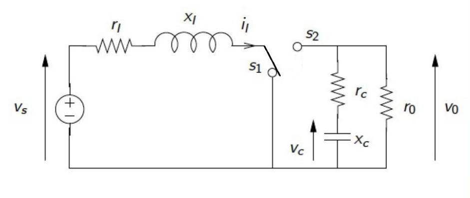

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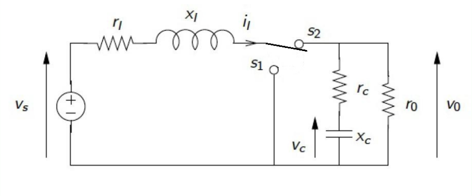

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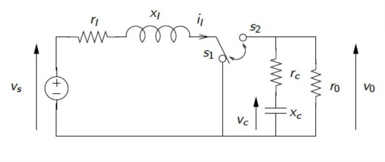

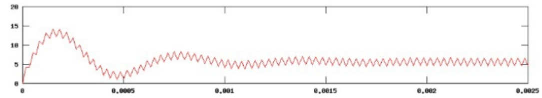

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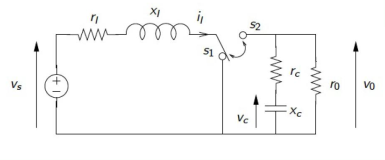

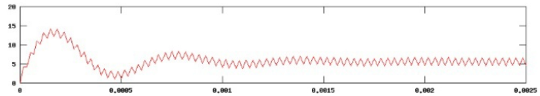

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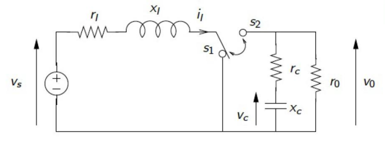

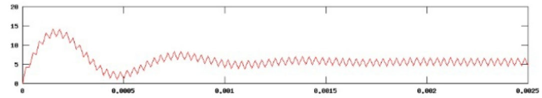

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NB: widespread in portable electronic devices (phones, laptops) supplied with batteries, which contain sub-circuits, each with its own voltage level requirement $\neq$ from that supplied by the battery

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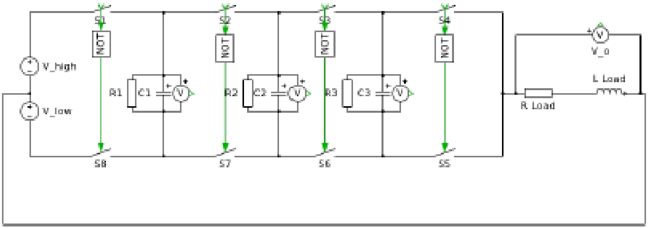
- Enables the use of renewable energy sources (photovoltaic, wind, and fuel cells can be easily interfaced to a MLC)
- Other advantage: can operate at low switching frequency ($\rightsquigarrow$ lower switching loss and stress, higher efficiency)

Principle of Multilevel Converters



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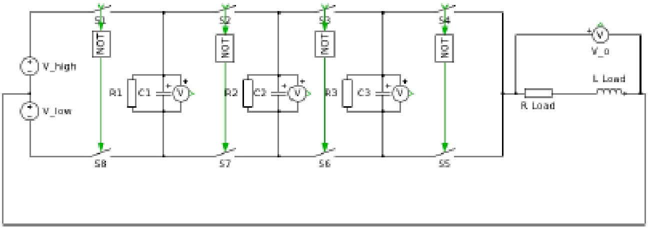

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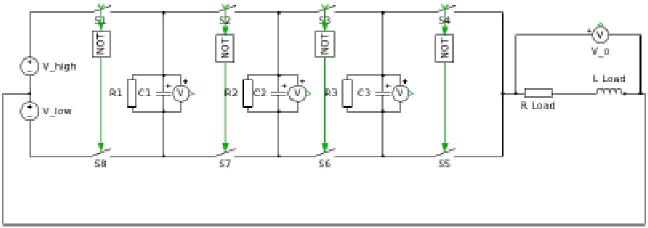

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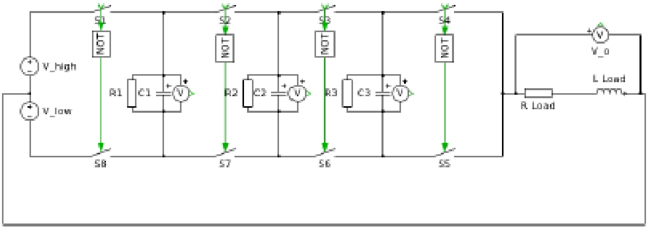

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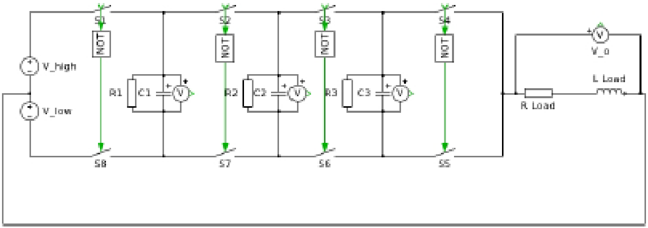

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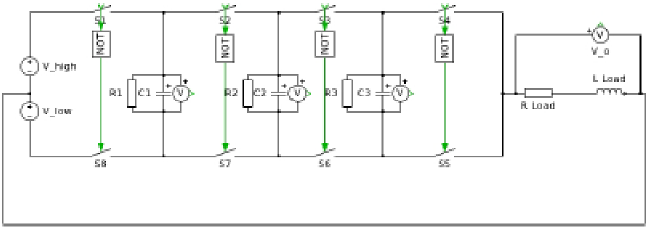

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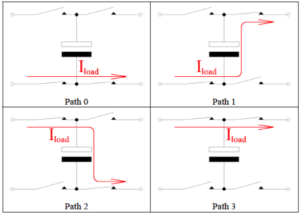
- according to the positions of the cells (mode), one is able to fraction the load voltage
- switching of modes occur periodically (sampling time τ)
- $\rightsquigarrow$ transform a DC voltage into a staircase waveform ($\approx$ sinusoidal)

Focus



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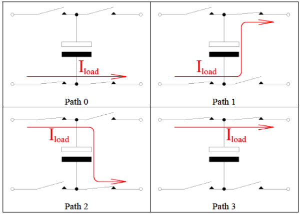
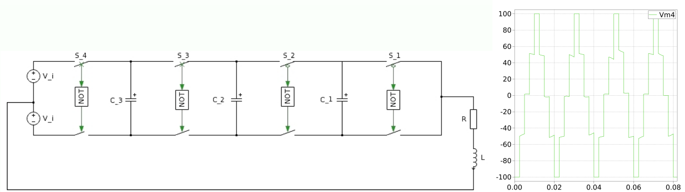


- According to the position of S_i and S_{i+1}, the capacitor C_i contributes or not to the output voltage.
- By global positioning of the switching cells, one is thus able to fraction the output voltage between $-v_i$ and $+v_i$.

Example: 5-level converter

- By controlling the modes at each sampling time, one can synthesize a 5-level staircase function



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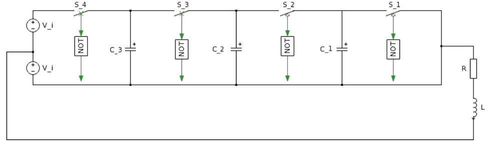

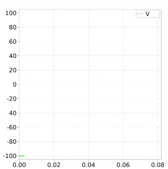

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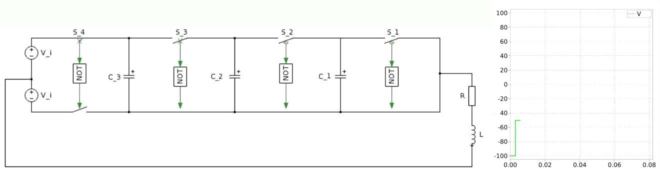

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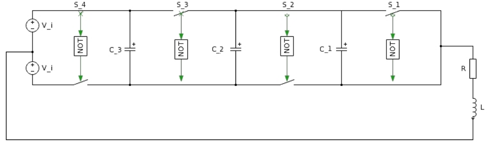

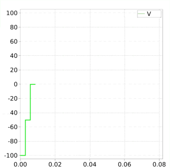

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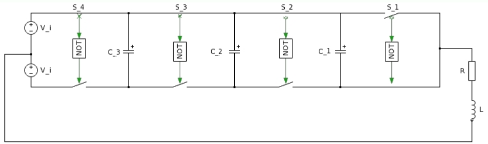

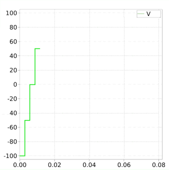

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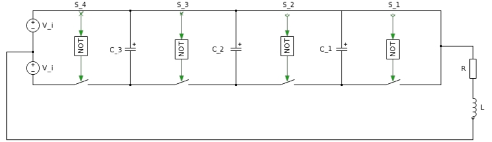

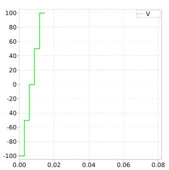

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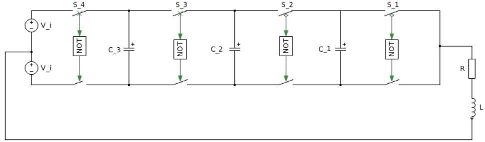

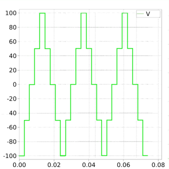

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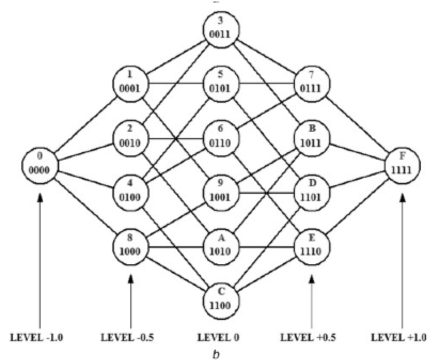

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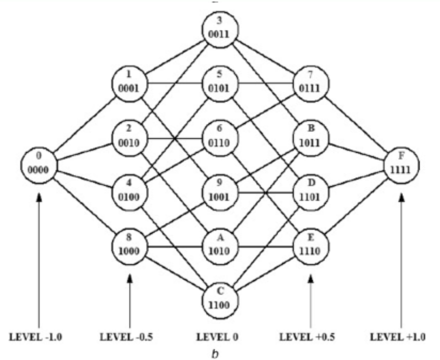

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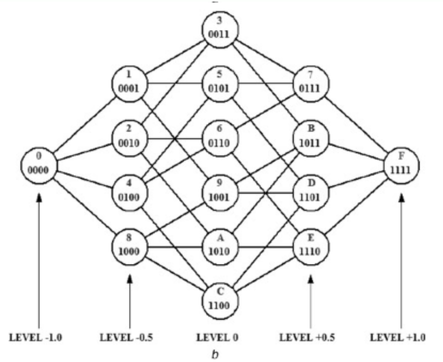

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- In industry, use of heuristic rules in order to find predefined sequences of patterns and apply them repeatedly (no formal guarantee of capacitor voltage balance property)

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The problem is to synthesize a safety controller for the switching system (correct-by-design controller)

Controllability of Switched Systems

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- duration of cycle $T = 8\tau$
- The 5-level converter can be seen as a switched system. Given a mode S, the associated dynamics is of the form $\dot{x}(t) = A_S x(t) + b_S$ with:

$$A_S = \begin{pmatrix} -\frac{1}{R_1C_1} & 0 & 0 & \frac{S_1-S_2}{C_1} \\ 0 & -\frac{1}{R_2C_2} & 0 & \frac{S_2-S_3}{C_2} \\ 0 & 0 & -\frac{1}{R_3C_3} & \frac{S_3-S_4}{C_3} \\ \frac{S_2-S_1}{L_{Load}} & \frac{S_3-S_2}{L_{Load}} & \frac{S_4-S_3}{L_{Load}} & -\frac{R_{Load}}{L_{Load}} \end{pmatrix} \quad b_S = \begin{pmatrix} 0 \\ 0 \\ 0 \\ \frac{(2S_1-1)v_{input}}{L_{Load}} \end{pmatrix}$$

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- If a fluctuation of $\pm 5V$ is admissible, the safety area is: $R = [145, 155] \times [95, 105] \times [45, 55]$

State Decomposition

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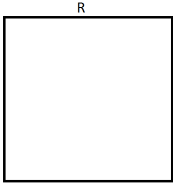

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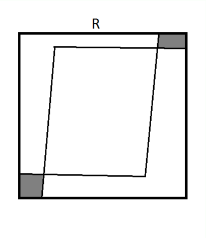

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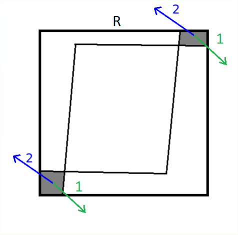

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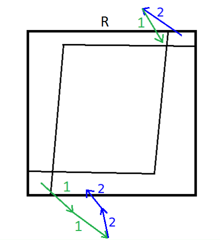
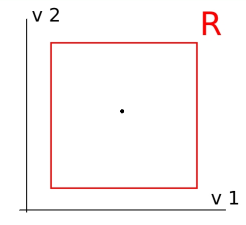


Sketch of the Decomposition Method

- Given a zone R



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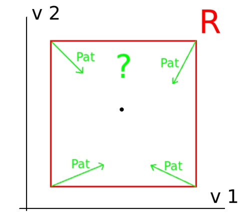

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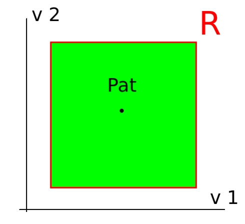

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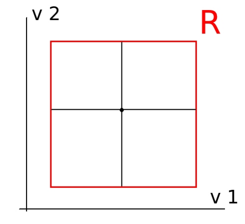

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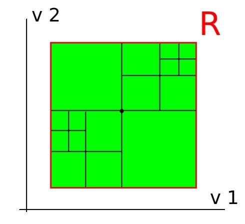

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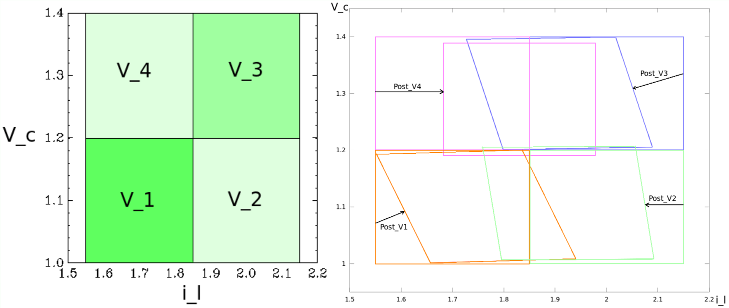

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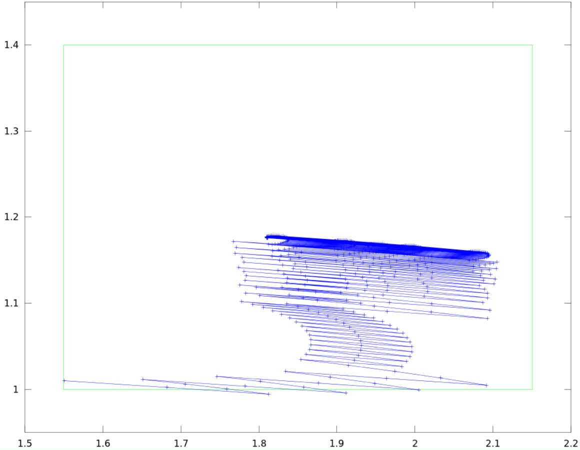
NB: The basic procedure can be refined with an extended safety set R^* in order to guarantee that all the intermediate points are in R^* at each sampling time.

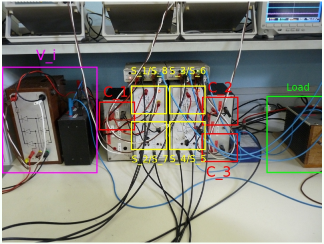
Trajectory under the induced control



Application to Multilevel Converters

Case Study: a Multilevel Converter

- A prototype built by SATIE Lab for the Farman project BOOST2



- The general function of a multilvel converter is to synthesize a desired AC voltage from several levels of DC voltages.

Application to Multilevel Converter (5 levels)

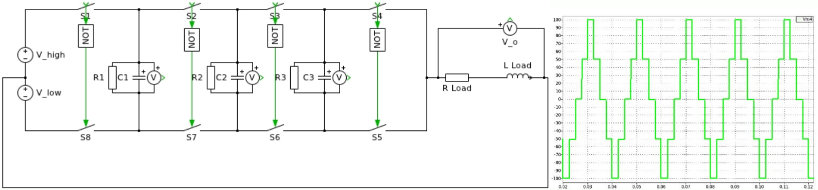


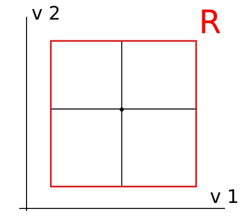
Figure : Electric scheme and ideal output for 5-level converter

Objective:

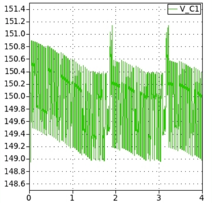
Find appropriate switching strategy in order to obtain the desired staircase output voltage while keeping capacitor voltage balancing

Application of Decomposition Procedure

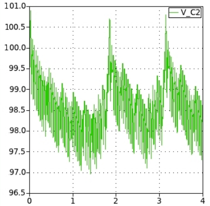
- $v_{input} = 100V$, $R_{load} = 50\Omega$, $C_1 = C_2 = C_3 = 0.0012F$, $L_{load} = 0.2H$, $R_1 = R_2 = R_3 = 20,000\Omega$, $T = 8\tau = 0.02s$ (frequency 50Hz)
- $R = [145, 155] \times [95, 105] \times [45, 55]$
  - procedure successful using only one bisection by dimension



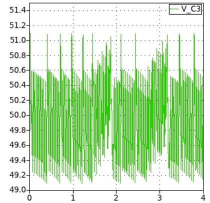
Numerical Simulations of the Capacitor Voltages



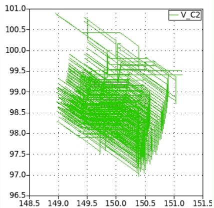
(a) $v_{C1} = f(t)$



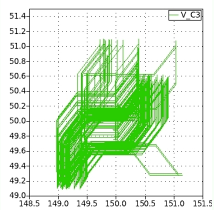
(b) $v_{C2} = f(t)$



(c) $v_{C3} = f(t)$



(d) projection on (v_{C1}, v_{C2})



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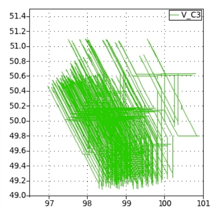
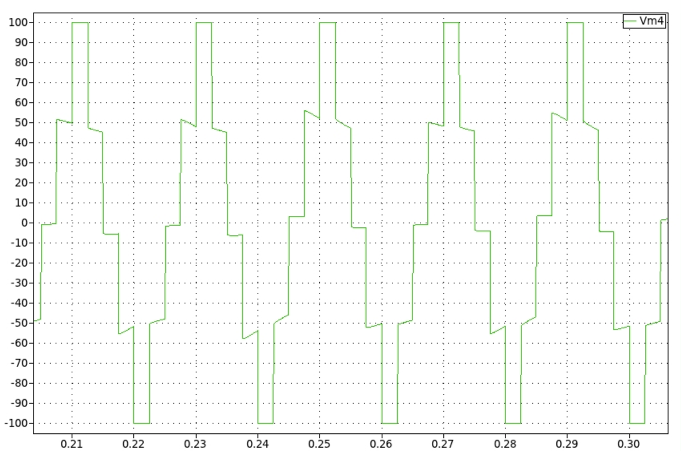


(f) projection on $v_{C2}, v_{C3})$

Numerical Simulation of the Output Voltage



Physical Experimentation on the Prototype

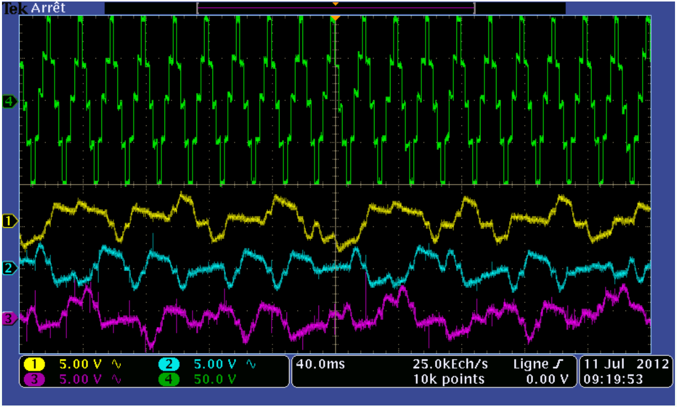


Figure : Output voltage and capacitor voltages

Correct-by-design control!

Other Results

- preliminary results about robustness on the prototype
- positive results also for multilevel with 7 levels
- prototype MINIMATOR available at
  https://bitbucket.org/ukuehne/minimator

Conclusion

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- Based on forward computation ($\leadsto$ better numerical stability for contractive systems)
- State-dependent control
- Successfully applied to physical prototype built by electrical engineering SATIE laboratory

Perspectives

- Improvement of the scalability of the approach (parallelization of the computations, e.g., GPU...)
- Refinement of the bisection method
- Addition of optimisation objectives
- Further work on robustness of the method in presence of variable resistive load.

Thanks!

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Questions?